What is claimed is:

1. A package structure with a cavity comprising:

a chip having a circuit disposed thereon and a plurality of first bonding pads disposed around the circuit, and the first bonding pads electrically connected to the circuit and an external circuit;

a multi-layer ceramic substrate having a cave formed thereon and a plurality of second bonding pads disposed around the cave, wherein the cave and the plurality of second bonding pads are corresponding to the circuit and the plurality of first bonding pads, respectively; and

an adhesive layer being substantially applied to the surface of the substrate, with the cave and the second bonding pads exposed from the adhesive layer, for tightly bonding the chip and the multi-layer ceramic substrate together such that the circuit of the chip is corresponding to the cave of the multi-layer ceramic substrate so as to form a cavity;

wherein the plurality of second bonding pads are respectively connected to a plurality of via conductors on the multi-layer ceramic substrate so as to connect with an external circuit.

2. The package structure with a cavity as claimed in claim 1, wherein the chip is a SAW chip, and the circuit is an interdigital transducer (IDT).

3. The package structure with a cavity as claimed in claim 1, wherein the chip is a semiconductor chip.

4. The package structure with a cavity as claimed in claim 1, wherein the chip is an optical chip.

5. The package structure with a cavity as claimed in claim 1, wherein the chip is a crystal chip.

6. The package structure with a cavity as claimed in claim 1, wherein the chip is a MEMS chip.

7. The package structure with a cavity as claimed in claim 1, wherein the material of the multi-layer ceramic substrate is selected from a group of AlN, low-temperature co-fired ceramic (LTCC), multi-layer co-fired ceramic (MLCC), AL_2O_3, and polymeric materials.

8. The package structure with a cavity as claimed in claim 1, wherein the plurality of first bonding pads are electrically connected to the plurality of second bonding pads by a gold layer.

9. The package structure with a cavity as claimed in claim 1 further comprising a buffer resin sealing and protecting the upper portion of the chip and the multi-layer ceramic substrate for stress relaxation and electrical insulation.

10. The package structure with a cavity as claimed in claim 9 further comprising a epoxy resin sealing and protecting the buffer resin for mechanical protection and enhancement of moisture resistance.